SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

A STEREO AUDIO SOLUTION FOR MULTIMEDIA APPLICATIONS USING TWO ST7546 A/D AND D/A CONVERTERS

ST7546 is a general-purpose signal processing Analog Front End, dedicated to full audio band applications.

ST7546 basically has to be connected to the serial interface of a DSP for data exchanges, and to a DAA (Data Access Arrangement) on analog side, which can be simply implemented as a differential to single ended amplifier on output and only an amplifier on signal input.

Main signals on the ST7546 host interface are :

- Din, data serial input : 16 bits per frame from DSP.
- Dout, data serial output : 16 bits per frame to the signal processor.
- FS, frame synchronisation provided to the host.
- SCLK, serial bit clock also provided to the processor, which is MCLK.
- NRESET, reset from host to ST7546.

The goal of note is to describe a simple way to manage at least two ST7546 Analog Front End from a single DSP.

Let's have a look on the startup sequence of the device from a reset pulse. The first FS falling edge will be generated after a number of cycles depending on the programmed value of N : 32 x N + offset as showned on Figure 1. So if data has to be sent just after reset the device, designer must take care of this delay.

Data word input/output are available after the falling edge of the Frame Synchronisation output of the device, and are sampled during the sixteen first cycles of clock after the frame synchronization signal.

So, to control a pair of ST7546, the DSP has to send and receive 32 bits words, where the first 16 bits are dedicated to the left audio channel, and second half to the right side for example. Each device must be synchronized on the NRESET signal provided by the signal processor.

A synchronous reset block is needed, where a single sequence of two sixteen MCLK cycles delayed signals NRESET1 and NRESET2, is gener-

Figure 1

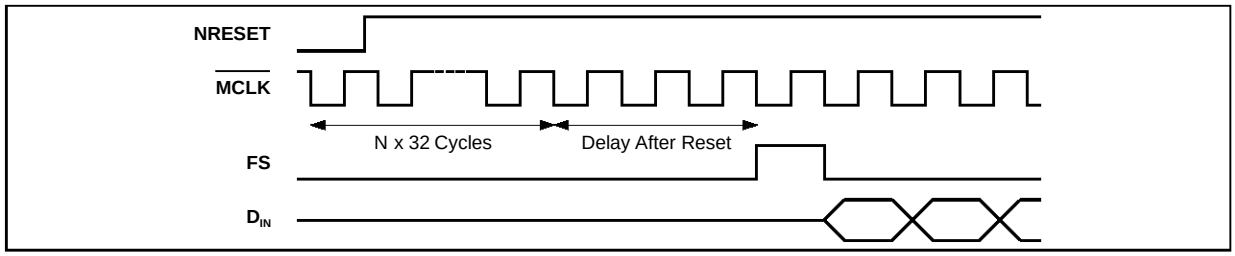
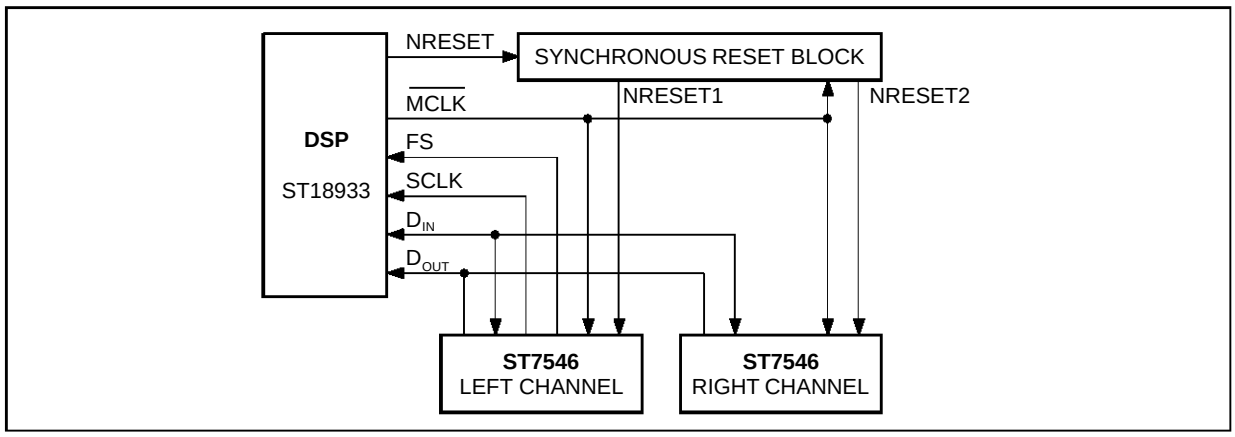


Figure 2



ated after the master reset NRESET (Figure 2). Both ST7546 are supposed to be in the same mode selected with HC0 and HC1 pins.

Figure 3 shows the phase delay between FS_left connected to the DSP, and FS_right.

For the processor, everything is like if there is a single interface on an hardware point of view ; the second ST7546 may be considered as a slave part. For correct control of data flow to dual ST7546 system, a burst must be generated by the processor as shown on Figure 4.

The synchronous reset block can be simply implemented with one synchronous 4 bits counter, two type D flip-flops, and three nand gates (Figure 5).

Figure 3

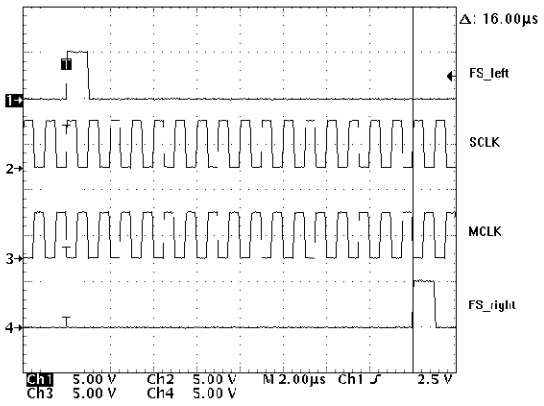


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Figure 4

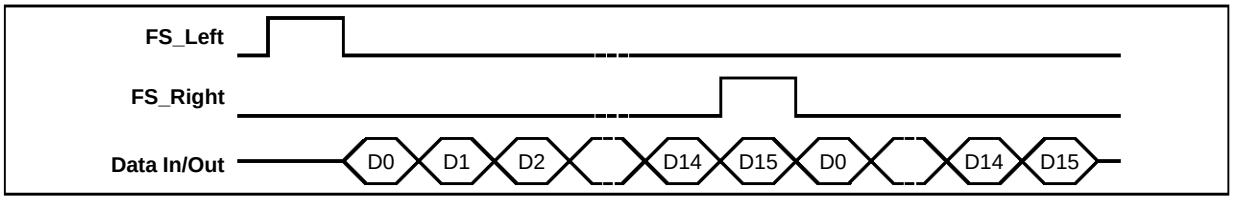

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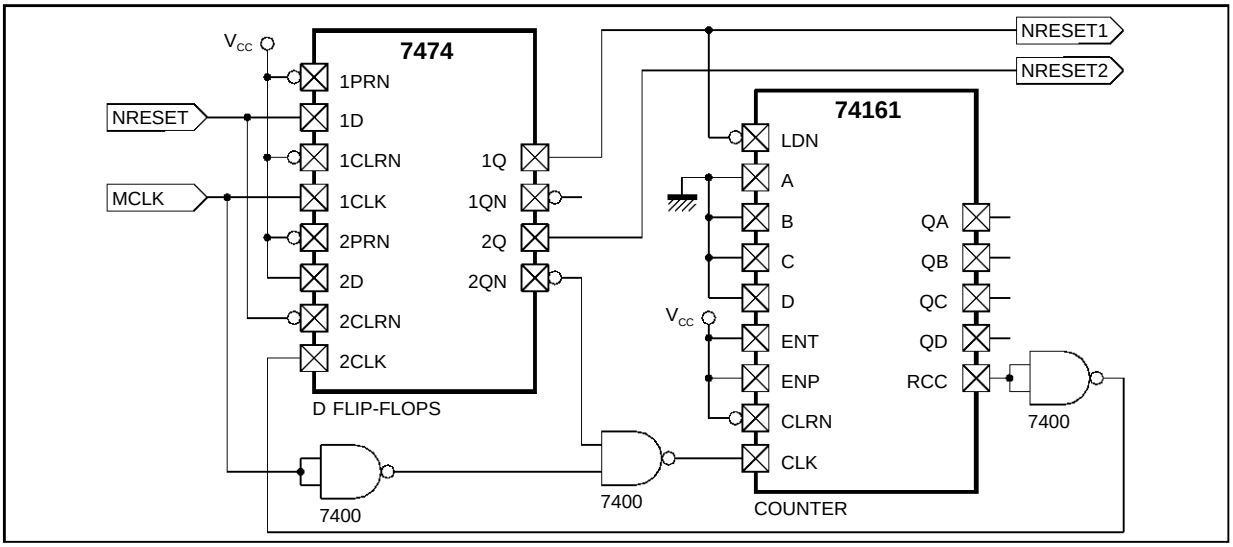
Figure 5



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